IN THE CLAIMS

Please amend the claims as follows:

Claims 1-14 (Canceled).

Claim 15 (Currently Amended): An image processing circuit of an image input device which performs a predetermined image processing of an image photographed by an image pickup device having a pixel array in said image input device, said circuit comprising:

a real time processing unit in which a predetermined general image processing of a pixel data in the image photographed by said image pickup device and inputted sequentially is performed by real time processing; and

a main memory disposed outside of said real time processing unit that stores a pixel data outputted from at least said real time processing unit, in image frame units, and stores defective pixel addresses in a pixel array sequence order having an order of the pixel array in said image input device, wherein

said real time processing unit further comprises a defective pixel compensation block that reads the defective pixel addresses stored in said main memory arranged in the pixel array sequence order, and performs defective pixel compensation when a pixel address of a pixel data residing in the image matches said defective pixel address, said defective pixel compensation performed in the pixel array sequence order, and

said defective pixel compensation block of said real time processing unit comprises a shift register with a plurality of registers connected in series, to which the defective pixel addresses stored in said memory are inputted sequentially and outputted sequentially.

Claim 16 (Currently Amended): The image processing circuit according to claim 15 wherein said defective pixel compensation block of said real processing unit further

comprises~~: a shift register with a plurality of registers connected in series, to which defective pixel addresses stored in said main memory are inputted sequentially,~~ a comparator connected to a rearmost stage of said shift register in which an address count value of a pixel data inputted sequentially is compared with a defective pixel address provided from said rearmost stage and, when a match is found, a defective pixel timing signal is outputted,

said shift register holds a defective pixel address, and output of said rearmost stage is looped to an input terminal of a foremost stage,

said comparator is a comparator in which an address count value of a pixel data inputted sequentially is compared with a defective pixel address provided from said rearmost stage and, when a match is found, a shift timing signal and a defective pixel timing signal are outputted, and

shift of said shift register is executed by said shift timing signal provided from said comparator.

Claims 17-27 (Canceled).

Claim 28 (Previously Presented): An image processing circuit of an image input device which performs a predetermined image processing of image photographed by an image pickup device in said image input device, said circuit comprising:

a real time processing unit in which a predetermined general image processing of a pixel data being photographed by said image pickup device and inputted sequentially is performed by real time processing; and

a main memory that stores a pixel data outputted from at least said real time processing unit, in image frame units, and wherein,

said real time processing unit further comprises a defective pixel compensation block that reads defective pixel addresses stored in said main memory disposed outside of said real time processing unit, and performs defective pixel compensation when a pixel address of a pixel data residing in image matches said defective pixel address, and when a plurality of defective pixel addresses are present in said main memory, said defective pixel addresses are stored in the order of a pixel array sequence,

said defective pixel compensation block of said real processing unit comprises

a shift register with a plurality of registers connected in series, to which defective pixel addresses stored in said main memory are inputted sequentially, and

a comparator connected to a rearmost stage of said shift register in which an address count value of a pixel data inputted sequentially is compared with a defective pixel address provided from said rearmost stage and, when a match is found, a defective pixel timing signal is outputted,

said shift register holds a defective pixel address, and output of said rearmost stage is looped to an input terminal of a foremost stage,

said comparator is a comparator in which an address count value of a pixel data inputted sequentially is compared with a defective pixel address provided from said rearmost stage and, when a match is found, a shift timing signal and a defective pixel timing signal are outputted, and

shift of said shift register is executed by said shift timing signal provided from said comparator.